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AMENDMENTS IN THE CLAIMS:

1. (Original) A controller for controlling the frame refresh rate of an active matrix display, characterised by comprising: a first circuit responsive to display signals from a display controller for supplying an enable signal (FE) for each Nth frame, where N is an integer greater than zero and is selectable from a plurality of values; and a second circuit for enabling refreshing of the display by each Nth frame supplied to the display controller in response to the enable signal (FE) and for preventing refreshing of the display by each other frame supplied to the display controller in the absence of the enable signal (FE).

2. (Currently Amended) ~~[A]~~ The controller as claimed in claim 1, characterised in that the display signals include frame ~~synchronisation~~ synchronization signals (VSYNC) and the first circuit is responsive to each Nth frame ~~synchronisation~~ synchronization signal (VSYNC).

3. (Currently Amended) ~~[A]~~ The controller as claimed in claim 1, characterised in that the first circuit is arranged to supply the enable signal (FE) for the duration of each Nth frame.

4. (Currently Amended) ~~[A]~~ The controller as claimed in claim 3, characterised in that the second circuit is arranged to connect the display to a power supply in response to the enable signal (FE) and to disconnect the display from the power supply in the absence of the enable signal (FE).

5. (Currently Amended) ~~[A]~~ The controller as claimed in claim 3, characterised in that the second circuit is arranged to gate at least one signal which influences power consumption of the display.

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6. (Currently Amended) ~~[A]~~ The controller as claimed in claim 5, characterised in that the second circuit comprises at least one gate for connection between the display controller and the display.

7. (Currently Amended) ~~[A]~~ The controller as claimed in claim 6, characterised in that the at least one gate comprises at least one logic gate.

8. (Currently Amended) ~~[A]~~ The controller as claimed in claim 6, characterised in that the at least one gate comprises at least one transmission gate.

9. (Currently Amended) ~~[A]~~ The controller as claimed in claim 5, characterised in that the second circuit is arranged to gate a memory read control signal (R') of the display controller.

10. (Currently Amended) ~~[A]~~ The controller as claimed in claim 5, characterised in that the at least one signal comprises a frame ~~synchronisation~~ synchronization signal from the display controller.

11. (Currently Amended) ~~[A]~~ The controller as claimed in claim 5, characterised in that the at least one signal comprises a line ~~synchronisation~~ synchronization signal from the display controller.

12. (Currently Amended) ~~[A]~~ The controller as claimed in claim 5, characterised in that the at least one signal comprises at least one image determining signal from the display controller.

13. (Currently Amended) ~~[A]~~ The controller as claimed in claim 1, characterised in that the first circuit includes means for fixing N at a value greater than one.

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14. (Currently Amended) ~~[A]~~ The controller as claimed in claim 1, characterised in that N is selectable from a plurality of predetermined values.

15. (Currently Amended) ~~[A]~~ The controller as claimed in claims 1, characterised in that the first circuit has an input (FC (1:N)) for selecting the value of N.

16. (Currently Amended) ~~[A]~~ The controller as claimed in claim 1, characterised in that the first circuit comprises a preloadable synchronous counter.

17. (Currently Amended) ~~[A]~~ The controller as claimed in claim 16, characterised in that the counter has a terminal count output (TC) for supplying the enable signal (FE).

18. (Currently Amended) ~~[A]~~ The controller as claimed in claim 17, characterised in that the counter has a load enable input (PE) connected to the terminal count output (TC).

19. (Currently Amended) ~~[A]~~ The controller as claimed in claim 16, characterised in that the counter has a clock input (CP) for receiving frame ~~synchronisation~~ synchronization signals (VSYNC) from the display controller.

20. (Currently Amended) ~~[A]~~ The controller as claimed in claim 1, characterised by a frame rate reduction enable input (FRC).

21. (Currently Amended) ~~[A]~~ The controller as claimed in claim 1, wherein the first circuit comprises a preloadable ~~synchoronous~~ synchronous counter and the counter has a count enable input arranged to be enabled by a rate reduction enable signal at a frame rate reduction enable input(FRC).

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22. (Currently Amended) ~~[A]~~ The controller as claimed in claim 21, characterised in that the count enable input (CEP) is connected ~~[ot]~~ to the enable input (FRC).

23. (Currently Amended) ~~[A]~~ The controller as claimed in claim 21, characterised in that the count enable input (CEP) is connected via a D-type latch (83) and a set/reset flip-flop to the enable input (FRC).

24. (Currently Amended) ~~[A]~~ The display controller characterised by including a frame refresh rate controller as claimed in claim 1.

25. (Currently Amended) ~~[A]~~ The display controller as claimed in claim 24, wherein the count enable input is connected via a D-type latch and a set/reset flip-flop to the enable input(FRC) and the enable input(FRC) is connected to receive a memory write control signal of the display controller and the first circuit comprises a preloadable ~~synchoronous~~ synchronous counter and the counter has a count enable input arranged to be enabled by a rate reduction enable signal at a frame rate reduction enable input(FRC).

26. (Original) An active matrix display characterised by including a controller as claimed in claim 1.

27. (Currently Amended) ~~[A]~~ The display as claimed in claim 26, characterised in that the second circuit of the controller is disposed adjacent an input of the display for receiving the display signals and is arranged to gate all of the display signals.

28. (Currently Amended) ~~[A]~~ The display as claimed in claim 26, characterised by comprising a plurality of data and scan driver integrated circuits, each of which includes a controller for controlling the frame refresh rate of an active matrix display, characterised by comprising: a first circuit responsive to display signals from a display

controller for supplying an enable signal (FE) for each Nth frame, where N is an integer greater than zero and is selectable from a plurality of values; and a second circuit for enabling refreshing of the display by each Nth frame supplied to the display controller in response to the enable signal (FE) and for preventing refreshing of the display by each other frame supplied to the display controller in the absence of the enable signal (FE).

29. (Currently Amended) ~~[A]~~ The display as claimed in claim 26, characterised by comprising a liquid crystal display.